WHAT IS CLAIMED IS:

1. A software/hardware language model conversion method for converting a first code described in a software description language to a second code described in a hardware description language, the method comprising:

converting the first code to the second code;

detecting a plurality of processes from the second code, the processes corresponding to a plurality of parallel procedures in the first code, which assign values to a predetermined shared variable; and

generating a value solving process for the detected processes corresponding to the parallel procedures, wherein the value solving process includes pairs of a data signal and an assignment timing signal from each of the detected processes as an input, and includes any one of data signals corresponding to a change of the assignment timing signal, as an output.

2. The method according to claim 1, wherein said second code includes a component hierarchical structure, wherein said value solving process includes a first value solving process which is generated at higher level in the component hierarchical structure and a second value solving process which is generated at lower level than that of the first value solving process, and further includes:

connecting the generated first and second value

solving processes each other.

3. The method according to claim 2, wherein the second value solving process outputs an assignment timing signal which is changed when a value of the data signal is updated to said first value solving process connected to the second value solving process, in addition to said data signal.

4. The method according to claim 2, further comprising:

connecting an input to the second value solving process to an input to the first value solving process; and

removing the second value solving process.

5. A software/hardware language model conversion method for converting a first code described in a software description language to a second code described in a hardware description language, the method comprising:

detecting a plurality of parallel procedures that assign values to a predetermined shared variable from the first code;

converting the first code to the second code; and

generating a value solving process for the detected processes corresponding to the parallel procedures, wherein the value solving process includes pairs of a data signal and an assignment timing signal from each of the detected processes as an input, and

includes any one of data signals corresponding to a change of the assignment timing signal, as an output.

6. The method according to claim 5, wherein said second code includes a component hierarchical structure, wherein said value solving process includes a first value solving process which is generated at higher level in the component hierarchical structure and a second value solving process which is generated at lower level than that of the first value solving process, and further includes:

connecting the generated first and second value solving processes each other.

7. The method according to claim 6, wherein the second value solving process outputs an assignment timing signal which is changed when a value of the data signal is updated to said first value solving process connected to the second value solving process, in addition to said data signal.

8. The method according to claim 6, further comprising:

connecting an input to the second value solving process to an input to the first value solving process; and

removing the second value solving process.

9. A software/hardware language model conversion method for converting a first code described in a software description language to a second code

described in a hardware description language, the method comprising:

converting the first code to the second code

detecting a plurality of processes from the second code, the processes corresponding to a plurality of procedures to call a predetermined parallel procedure; and

generating a procedure call solving process which exclusive controls a call operation to the parallel procedure by the detected process, wherein the procedure call solving process includes pairs of an call timing signal and an argument data signal, from each of the detected processes, as an input, and includes terminal signal and a return value signal, as an output to the processes, from the called procedure.

10. The method according to claim 9, wherein said second code includes a component hierarchical structure, wherein said procedure call solving process includes a first procedure call solving process which is generated at higher level in the component hierarchical structure and a second procedure call solving process which is generated at lower level than that of the first procedure call solving process, and further includes:

connecting the generated first and second procedure call solving processes each other.

11. The method according to claim 10, further

comprising:

connecting an input to the second procedure call solving process to an input to the first procedure call solving process; and

removing the second procedure call solving process.

12. A software/hardware language model conversion method for converting a first code described in a software description language to a second code described in a hardware description language, the method comprising:

detecting a plurality of procedures from the first code, which call a predetermined parallel procedure;

converting the first code to the second code; and

generating a procedure call solving process which exclusive controls an operation of a plurality of processes corresponding to the detected procedures, wherein the procedure call solving process includes pairs of a call timing signal and an argument data signal from each of the detected processes, as an input, and includes a terminal signal and a return value signal, as an output to the processes, from the called procedure.

13. The method according to claim 12, wherein said second code includes a component hierarchical structure, wherein said procedure call solving process includes a first procedure call solving process which

is generated at higher level in the component hierarchical structure and a second procedure call solving process which is generated at lower level than that of the first procedure call solving process, and further includes:

connecting the generated first and second procedure call solving processes each other.

14. The method according to claim 13, further comprising:

connecting an input to the second procedure call solving process to an input to the first procedure call solving process; and

removing the second procedure call solving process.

15. A software/hardware language model conversion method for converting a first code described in a software description language to a second code described in a hardware description language, the method comprising:

converting the first code to the second code;

detecting a plurality of processes from the second code, the processes corresponding to a plurality of parallel procedures in the first code, which assign values to a predetermined shared variable;

generating a value solving process for the detected processes corresponding to the parallel procedures, wherein the value solving process includes

pairs of a data signal and an assignment timing signal from each of the detected processes, as an input, and includes any one of data signals corresponding to a change of the assignment timing signal, as an output;

converting the value solving process relating to a procedure call between parallel programs to a procedure call solving process wherein the procedure call solving process includes pairs of an call timing signal and an argument data signal from each of the detected processes, as an input, and includes terminal signal and a return value signal, as an output to the processes, from the called procedure.

16. A software/hardware language model conversion method for converting a first code described in a software description language to a second code described in a hardware description language, the method comprising:

detecting a plurality of parallel procedures that assign values to a predetermined shared variable from the first code;

converting the first code to the second code;

generating a value solving process for the detected processes corresponding to the parallel procedures, wherein the value solving process includes pairs of a data signal and an assignment timing signal from each of the detected processes, as an input, and includes any one of data signals corresponding to a

change of the assignment timing signal, as an output, the data signal indicating a value of the shared variable; and

converting the one of the value solving process relating to a procedure call between parallel programs to a procedure call solving process, wherein the procedure call solving process includes pairs of a call timing signal and an argument data signal from each of the detected processes, as an input, and includes a terminal signal and a return value signal, as an output to the processes, from the called procedure.

17. A computer program product comprising:

a computer storage medium and a computer program code mechanism embedded in the computer storage medium for causing a computer to convert a first code described in a software description language to a second code described in a hardware description language, the computer code mechanism comprising:

a computer code device configured to convert the first code to the second code;

a computer code device configured to detect a plurality of processes from the second code, the processes corresponding to a plurality of parallel procedures in the first code, which assign values to a predetermined shared variable; and

a computer code device configured to generate a value solving process for the detected processes

corresponding to the parallel procedures, wherein the value solving process includes pairs of a data signal and an assignment timing signal from each of the detected processes as an input, and includes any one of data signals corresponding to a change of the assignment timing signal, as an output.

18. The computer program product according to claim 17, wherein said second code includes a component hierarchical structure, wherein said value solving process includes a first value solving process which is generated at higher level in the component hierarchical structure and a second value solving process which is generated at lower level than that of the first value solving process, and further includes:

a computer code device configured to connect the generated first and second value solving processes each other.

19. The computer program product according to claim 18, wherein the second value solving process outputs an assignment timing signal which is changed when a value of the data signal is updated to said first value solving process connected to the second value solving process, in addition to said data signal.

20. The computer program product according to claim 18, further comprising:

a computer code device configured to connect an input to the second value solving process to an input

to the first value solving process; and

a computer code device configured to remove the second value solving process.

A1

21. A computer program product comprising:

a computer storage medium and a computer program code mechanism embedded in the computer storage medium for causing a computer to convert a first code described in a software description language to a second code described in a hardware description language, the computer code mechanism comprising:

a computer code device configured to detect a plurality of parallel procedures that assign values to a predetermined shared variable from the first code;

a computer code device configured to convert the first code to the second code; and

a computer code device configured to generate a value solving process for the detected processes corresponding to the parallel procedures, wherein the value solving process includes pairs of a data signal and an assignment timing signal from each of the detected processes as an input, and includes any one of data signals corresponding to a change of the assignment timing signal, as an output.

22. The computer program product according to claim 21, wherein said second code includes a component hierarchical structure, wherein said value solving process includes a first value solving process which is

generated at higher level in the component hierarchical structure and a second value solving process which is generated at lower level than that of the first value solving process, and further includes:

A1

a computer code device configured to connect the generated first and second value solving processes each other.

23. The computer program product according to claim 22, wherein the second value solving process outputs an assignment timing signal which is changed when a value of the data signal is updated to said first value solving process connected to the second value solving process, in addition to said data signal.

24. The computer program product according to claim 22, further comprising:

a computer code device configured to connect an input to the second value solving process to an input to the first value solving process; and

a computer code device configured to remove the second value solving process.

25. A computer program product comprising:

a computer storage medium and a computer program code mechanism embedded in the computer storage medium for causing a computer to convert a first code described in a software description language to a second code described in a hardware description language, the computer code mechanism comprising:

a computer code device configured to convert the first code to the second code

a computer code device configured to detect a plurality of processes from the second code, the processes corresponding to a plurality of procedures to call a predetermined parallel procedure; and

a computer code device configured to generate a procedure call solving process which exclusive controls a call operation to the parallel procedure by the detected process, wherein the procedure call solving process includes pairs of an call timing signal and an argument data signal, from each of the detected processes, as an input, and includes terminal signal and a return value signal, as an output to the processes, from the called procedure.

26. The computer program product according to claim 25, wherein said second code includes a component hierarchical structure, wherein said procedure call solving process includes a first procedure call solving process which is generated at higher level in the component hierarchical structure and a second procedure call solving process which is generated at lower level than that of the first procedure call solving process, and further includes:

a computer code device configured to connect the generated first and second procedure call solving processes each other.

27. The computer program product according to claim 26, further comprising:

a computer code device configured to connect an input to the second procedure call solving process to an input to the first procedure call solving process; and

a computer code device configured to remove the second procedure call solving process.

28. A computer program product comprising:

a computer storage medium and a computer program code mechanism embedded in the computer storage medium for causing a computer to convert a first code described in a software description language to a second code described in a hardware description language, the computer code mechanism comprising:

a computer code device configured to detect a plurality of procedures from the first code, which call a predetermined parallel procedure;

a computer code device configured to convert the first code to the second code; and

a computer code device configured to generate a procedure call solving process which exclusive controls an operation of a plurality of processes corresponding to the detected procedures, wherein the procedure call solving process includes pairs of a call timing signal and an argument data signal from each of the detected processes, as an input, and includes a terminal signal

and a return value signal, as an output to the processes, from the called procedure.

29. The computer program product according to claim 28, wherein said second code includes a component hierarchical structure, wherein said procedure call solving process includes a first procedure call solving process which is generated at higher level in the component hierarchical structure and a second procedure call solving process which is generated at lower level than that of the first procedure call solving process, and further includes:

a computer code device configured to connect the generated first and second procedure call solving processes each other.

30. The computer program product according to claim 29, further comprising:

a computer code device configured to connect an input to the second procedure call solving process to an input to the first procedure call solving process; and

a computer code device configured to remove the second procedure call solving process.

31. A computer program product comprising:

a computer storage medium and a computer program code mechanism embedded in the computer storage medium for causing a computer to convert a first code described in a software description language to a

second code described in a hardware description language, the computer code mechanism comprising:

a computer code device configured to convert the first code to the second code;

A1

a computer code device configured to detect a plurality of processes from the second code, the processes corresponding to a plurality of parallel procedures in the first code, which assign values to a predetermined shared variable;

a computer code device configured to generate a value solving process for the detected processes corresponding to the parallel procedures, wherein the value solving process includes pairs of a data signal and an assignment timing signal from each of the detected processes, as an input, and includes any one of data signals corresponding to a change of the assignment timing signal, as an output;

a computer code device configured to convert the value solving process relating to a procedure call between parallel programs to a procedure call solving process wherein the procedure call solving process includes pairs of an call timing signal and an argument data signal from each of the detected processes, as an input, and includes terminal signal and a return value signal, as an output to the processes, from the called procedure.

32. A computer program product comprising:

a computer storage medium and a computer program code mechanism embedded in the computer storage medium for causing a computer to convert a first code described in a software description language to a second code described in a hardware description language, the computer code mechanism comprising:

a computer code device configured to detect a plurality of parallel procedures that assign values to a predetermined shared variable from the first code;

a computer code device configured to convert the first code to the second code;

a computer code device configured to generate a value solving process for the detected processes corresponding to the parallel procedures, wherein the value solving process includes pairs of a data signal and an assignment timing signal from each of the detected processes, as an input, and includes any one of data signals corresponding to a change of the assignment timing signal, as an output, the data signal indicating a value of the shared variable; and

a computer code device configured to convert the one of the value solving process relating to a procedure call between parallel programs to a procedure call solving process, wherein the procedure call solving process includes pairs of a call timing signal and an argument data signal from each of the detected processes, as an input, and includes a terminal signal

and a return value signal, as an output to the processes, from the called procedure.